Remarks

Applicant thanks Examiner Mandala for his careful examination and clear explanation of the objections and rejections. In response, Applicant amends the specification and cancels claims 1-6. Applicant respectfully submits that, as amended, the application is in allowable form and the claims are distinguishable from the reference for the reasons set forth in the following sections.

1. The gate element in claim 7 is fully supported in the description and in the drawings.

   Applicant respectfully submits that 'the gate structure' is fully explained in the specification[1], and in the drawing Figures 3 and 4. In paragraph 1, it is referred as 'the gate', and in paragraph 4 it is referred as 'a gate structure'. It is well known by a person skilled in art of solid-state device that both these terms refer to the gate element of a MOS and an FET device.

2. The §112, second paragraph rejection against claim 7 is improper because the term 'sublithographic' is not indefinite.

   The Office action rejects 'sublithographic' as a general concept and as indefinite. Applicant respectfully submits that the test for definiteness under 35 U.S.C. §112, second paragraph is whether "those skilled in the art wound understand what is claimed when the claim is read in light of the specification."[2] If the claims, read in the light of the specifications, reasonably apprise those skilled in the art both of the utilization and scope of the invention, and if the language is as precise as the subject matter permits, the courts can demand no more.[3]

   In the present invention, the term 'sublithographic' refers to a dimension that is smaller than what is possible with lithographic technology at the time of the invention[4]. As Examiner Mandala alludes, the wavelength of the exposure light is a variable and changes

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[1] See p.9, paragraphs 1 and 4.

[2] Orthokinetics, Inc. v. Safety Travel Chairs, Inc., 806 F.2d 1565, 1576, 1 USPQ2d 1081, 1088 (Fed. Cir. 1986).

[3] Shatterproof Class Corp. v. Libbey-Ovens Ford Co., 758 F.2d 613, 225 USPQ 634 (Fed. Cir. 1985)

[4] See, p.10, l.14.

with lithographic technology. Since the device described in claim 1 is independent of a specific lithographic technology, using the term 'sublithographic' is as precise as the subject matter permits in order to satisfies requirement of §112, second paragraph.

3. The judicially created doctrine of obviousness-type double patenting rejection against claim 1 is improper because the claims in the present invention differ from the claims in the reference and there is no evidence of obviousness.

The Office action failed to support the rejection against claim 7 with any obviousness evidence. Besides, the transistor described in claims 1 & 5-6 of U.S. Patent 5,043,535 lacks at least one element in claim 1 of the present invention so claim 1 can not be broader than the cited claims in the reference.

The cited claims 1 and 5-6 teach a transistor that has the following elements:

(a) a drain region;

(b) a source region opposite the drain region;

(c) a channel region between the drain and source regions in a first substrate layer;

(d) a front gate;

(e) a self-aligned implant region below the channel, aligned with the front gate and having a width approximately equal that of the front gate and the distance between the sidewall spacers;

(f) a buried dielectric layer below the first substrate layer and in which the self-aligned implant region is embedded. The self-aligned region is either a back gate or a back body contact comprises of polysilicon.

The claim 7 describes an integrated circuit structure that includes the following elements and limitations:

(a) a gate structure formed on a body of semiconductor material;

(b) an insulating layer formed opposite the gate structure beneath the semiconductor material;

(c) a conducting region within the insulating layer, beneath the gate structure; and

(d) the conducting region having sublithographic width.

At least the limitation (d) is lacking in the claims of the reference. In the referred claims, the self-aligned region is to have a width approximately equal that of the front gate. The dimension of the front gate is not limited to the minimum design rule – it could be larger than the lithographic limit, depending on the transistor-performance requirement. In the claim 7 of the present invention, however, the conducting region is limited to having sublithographic width. The scope of claim 7 is therefore narrower, rather than broader, than that of the transistor in the reference in this regard.

It is clear that the scope of claim 1 and that of the transistor in the reference are distinguishable. There is no teaching or suggesting in the reference to combine the transistor with the limitation in claim 1 of the present invention. Therefore, Applicant respectfully submits that the double patenting rejection is improper.

Claims 9 and 11 depend on claim 7 with further limitations. Therefore, the double patenting rejection against claims 9 and 11 are also improper.

4. Claim 7 is not anticipated by U.S. Patent No. 6,043,535 because it does not teach at least one element in claim 7.

One limitation of claim 7 is that the conducting region having sublithographic width. As explained in the previous paragraph, the reference teaches a transistor with a self-aligned region that is approximately equal that of the front gate. It is well known in the art of integrated circuit design that for various reasons, transistors of various gate lengths – many greater than lithographic limit – are often included in integrated circuits. Therefore, a transistor with a self-aligned region that is equal that of the front gate can not be said to anticipate a conducting region having sublithographic width.

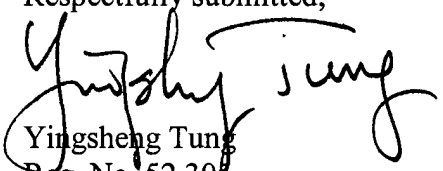
5. Claims 8, 9, 10, and 11 are not anticipated by U.S. Patent No. 6,043,535 because they depend on claim 7 and with further limitations.

In particular, claim 8 further limits the conducting region to contact the semiconductor material; claim 9 further limits the conducting region to be formed in a trench with sidewalls; claim 10 further limits the semiconductor material to silicon; and claim 11 further limits the conducting region to be separated from the semiconductor material by a dielectric material.

In conclusion, Applicant respectfully submit that the gate structure element in claim 7 is fully supported in the original description and in the original drawings; the term sublithographic is not indefinite; the claims in the present invention and those in the cited reference have distinguishable scope, the claims in the present invention are not broader than those in the reference and the Office action did not provide any prima facie evidence of obviousness; and the reference does not anticipate because it does not teach at least one limitation in all claims of the present invention.

Applicants respectfully request withdrawing of the rejections and further examination of this application.

Respectfully submitted,



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